cont'd AS

insulating, the wiring shape is different between a signal line and a ground line or between a signal line and an electric source line. --

REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

This amendment is in response to the Office Action dated December 13, 2001.

By the present amendment, the claims have been amended to respond to the claim objections and 35 U.S.C. 112 rejections set forth in the Office Action. Also, the drawings have been amended to respond to certain points of objection raised in the Office Action.

Briefly, the present invention is directed to an improved wafer process package which includes a stress relaxation layer to reduce stress between a semiconductor chip and a circuit board (e.g., noting that an example of such a stress relaxation layer is shown by the numeral 5 in Fig. 1). An important feature of the present invention is that the stress relaxation layer is made of thermoplastic resin. Prior to the present invention, thermosetting resin was used as a stress relaxation layer in previous wafer process packages. As discussed on page 31, beginning on line 21, by virtue of using a thermoplastic resin, applicants are able to form a protrusive portion such as indicated by the numeral 34 at the

edges of the stress relaxation layer in Fig. 9. As noted on page 32, line 20 et seq., this protrusive portion provides a flexible portion along the wiring which can help in preventing breakage of the wiring 4. The advantage of using thermoplastic resin rather than thermosetting resin to form the protrusive region 34 as specifically discussed on page 64, line 25 et seq. Another advantage of using a thermoplastic resin is that it is easy to make the protrusive portions 34 by a printing process such as described on page 65.

Reconsideration and removal of the objection to the drawings on page 2 of the Office Action is respectfully requested. With regard to the first paragraph of the objection concerning the width of the wirings, it is noted that these features are shown already in Figs. 14-16. With regard to the objection to the drawings for not showing the material E described on page 64, line 2, Figs. 22A, 22B, 23A, 23B, and 23C have each been labeled to particularly identify the material that they refer to, as described in the specification on page 59, line 28 through page 60, line 4. As for the objection on the last paragraph of page 2 of the Office Action, it is noted that each of the numerals 4, 9, 10, 33 and 5 are particularly mentioned already in the specification. As such, the use of the numeral 4a in Fig. 16 is clearly understandable by the identification of (signal line) in the drawing figure as one type of redistributing wire 4 shown in Fig. 1 and discussed, for example, on page 18, line

25 et seq. In light of the description of the respective numerals already found in the specification, it is respectfully submitted that no drawing correction is necessary, and that those reading the specification in light of the drawings will clearly understand the intended meaning of the numerals mentioned. Accordingly, reconsideration and removal of this objection is respectfully requested.

Reconsideration and removal of the claim objections set forth on page 3 of the Office Action is also respectfully requested. Each of claims 1, 6, 12 and 13 has been amended to clarify the language questioned in the claim objections. Accordingly, reconsideration and removal of these objections is also respectfully requested.

Reconsideration and removal of the 35 U.S.C. 112, second paragraph, rejection set forth on page 3 of the Office Action is also respectfully requested. Each of claims 1, 2, 3, 4, 10 and 12 have been amended to provide antecedent basis for the terminology questioned. Accordingly, removal of this rejection is also respectfully requested.

Reconsideration and removal of the rejection of claims 1-14 over the cited U.S. Patent 6,313,532 to Shimoishizaka is also respectfully requested. By the present amendment, independent claim 12 has been amended to define that the stress relaxation layer is made of a thermoplastic resin. This limitation is already found in independent claim 1. Although the Office Action is premised on the stress

relaxation layer of Shimoishizaka being a thermoplastic resin, in fact, there is nothing in the reference that suggests this. The stress relaxation layer in Shimoishizaka is the low elasticity layer 20 which "absorbs thermal stress and the like caused in heating or cooling the semiconductor device," as described in the abstract of Shimoishizaka. In column 6, line 7 et seq. it is stated:

> "a low elasticity layer 20 of an insulating material with a low elastic modulus is formed an area excluding the electrode arranging area."

However, there is nothing in Shimoishizaka which suggests that this low elasticity layer 20 is a thermoplastic resin. As such, it is respectfully submitted that both the independent claims 1 and 12 clearly define over Shimoishizaka inasmuch as this reference completely fails to teach or suggest the formation of a stress relaxation layer of thermoplastic resin.

Beyond this, dependent claims such as claim 2 and the new claim 17 et seq. describe a protuberant portion such as that shown in Fig. 9 of the present application by the numeral 34. As noted in the above discussion, this protuberant portion is important in providing extra slack to assist in preventing wire breakage. This feature is completely lacking in the Shimoishizaka reference. Accordingly, particular consideration and allowance of these dependent claims is respectfully requested.

Other dependent claims contain further features which are

neither taught nor suggested by Shimoishizaka. For example, claim 4 particularly defines the feature of the melting temperature of the thermoplastic resin of the stress relaxation layer which is not at all suggested in the Shimoishizaka reference. Similarly, the glass transition temperatures set forth in claim 5 for the thermoplastic resin is not at all suggested in Shimoishizaka (noting that this feature is also found in independent claim). Dependent claim 10 defines featurings of the wiring width which are also not at all suggested in Shimoishizaka, particularly when considered in combination with the features of the parent claims 1 or 2. For these reasons, reconsideration and allowance of the dependent claims of the present application is also respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with markings to show changes made."

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of, either by telephone discussion or by personal interview, the Examiner is invited to contact applicants' undersigned attorney at the number indicated below.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this

paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus, Deposit Account No. 01-2135 (500.39919X00).

Respectfully submitted,

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703/312-6600

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claims 15 and 16 have been cancelled without prejudice.

Claims 1-6, 8, 10, 12, and 13 have been amended as follows:

1. (Amended) A semiconductor device comprising:

a semiconductor element having a circuit surface on which a plurality of circuit electrodes are disposed, said circuit surface being coated with a protecting film,

a stress relaxation layer which is formed on the protecting film of the circuit surface of said semiconductor element so as to expose the circuit electrodes, is made of a [cured] thermoplastic resin and has an inclination in [the] an edge portion thereof to form an inclined edge portion,

a wiring layer [consisting] comprised of a plurality of wirings, each of said wirings being connected to one of the circuit electrodes and disposed so as to make an electrical connection from said circuit [electrode] electrodes, via the edge portion of the stress relaxation layer and to a desired site on [the] a surface of the stress relaxation layer,

a surface protecting film which covers [the] a

surface of the wiring layer so as to expose a prescribed portion on each of the plurality of wirings on the surface of the stress relaxation layer, and

an external connection terminal formed by connecting a bump to said prescribed exposed portion of each of the plurality of wirings.

2. (Amended) A semiconductor device according to Claim 1, wherein a [swelling] protuberant portion is formed in [the] a surrounding part connected to the inclined edge portion of the stress relaxation layer and a deflected portion is formed in the wiring existing on said [swelling] protuberant portion.

3. (Amended) A semiconductor device according to Claim 1 or 2, wherein [the] a melting temperature Tm of the [cured] thermoplastic resin in said stress relaxation layer is not lower than the maximum attainable temperature Tmax in the process of forming said wiring layer and surface protecting layer.

4. (Amended) A semiconductor device according to Claim 1 or 2, wherein [the] a melting temperature Tm of the [cured] thermoplastic resin in the stress relaxation layer is not lower than 350°C.

5. (Amended) A semiconductor device according to Claim 1 or

2, wherein glass transition temperature Tg of the [cured] thermoplastic resin in said stress relaxation layer is in the range of from 150°C to 400°C.

6. A semiconductor device according to Claim 1 or 2, wherein a coefficient of thermal expansion of the [cured] thermoplastic resin in said stress relaxation layer is not greater than 200 ppm/°C.

8. A semiconductor device according to Claim 1 or 2, wherein the [cured] thermoplastic resin in said stress relaxation layer is at least one member selected from the group consisting of polyimide, polyamide, polyamide-imide, epoxy, phenolic and silicone.

10. (Amended) A semiconductor device according to Claim 1 or 2, wherein the wirings are formed so that [the] a width of the wiring in the edge portion of said stress relaxation layer is greater than the width of wiring in [the] a flat portion of said stress relaxation layer, at least regarding signal wirings.

12. (Amended) A semiconductor device comprising:

a semiconductor element having a plurality of circuit electrodes disposed thereon and a circuit surface coated with a protecting film,

a stress relaxation layer formed on the protecting film of the circuit surface of said semiconductor element so as to expose the circuit electrodes, which is made of a [cured] thermoplastic resin having a glass transition temperature Tg falling in the range of from 150°C to 400°C and has an inclination in [the] an edge portion thereof,

a wiring layer [consisting] comprised of a plurality of wirings, each of said wirings being connected to one of the circuit electrodes and disposed so as to make [en] an electrical connection from said circuit electrode, via the edge portion of stress relaxation layer and to a desired site on [the] a surface of the stress relaxation layer,

a surface protecting film which covers [the] a surface of the wiring layer so as to expose a prescribed portion on each of the plurality of wirings on the surface of the stress relaxation layer, and

an external connection terminal formed by connecting a bump to said prescribed exposed portion of each of the plurality of exposed wirings.

13. (Amended) A semiconductor device according to Claim 12, wherein a thickness of said stress relaxation layer is in the range of from about 35 μm to about 150 μm.

New claims 17-28 have been added.